Remarks:

These remarks are responsive to the Office action dated December 20, 2004. Prior to the entry of this amendment, claims 1-29 and 34-46 remained pending in the application. Claims 30-33 previously were cancelled pursuant to an earlier restriction requirement.

In connection with the present Office action, applicant notes, with appreciation, that the Examiner has allowed claims 34-38, and has indicated that claims 4-22, 26, 27, 28 and 41-46 would be allowable if rewritten in independent form to include the base claim and any intervening claims.

By this amendment, applicant has amended claims 4, 26, 28 and 41 to place such claims in independent form, as suggested by the Examiner. Claims 4, 26, 28 and 41 thus are understood to be in allowable form. Claims 5-22, 27 and 42-46 depend from newly independent claims 4, 26 and 41, and thus also are understood to be in allowable form.

Claim 40 has been cancelled without prejudice.

Rejections under 35 U.S.C. § 103(a)

Claims 1-3, 23-25, 29, 39, and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang et al. (US 4,598,305) in view of Makita et al. (US 5,936,291). Applicant respectfully disagrees, and asserts that the Examiner has not established *prima facie* obviousness of the claims.

Claims 1-3, 23

Claim 1 recites a thin film transistor including source, drain, and gate electrodes, "a deposited thin-film channel region having a portion doped with an impurity to change the fixed charge density within the portion relative to a remainder

of the channel region and disposed between the source and drain electrode," and "a dielectric material electrically separating the gate electrode from the channel region. Claims 2-3 and 23 depend from claim 1.

Chiang et al. relates to a thin film transistor containing a "p-n junction located parallel to the surface of the substrate" (col. 2, lines 34-35). Chiang et al. discloses the creation of such a structure by separately introducing donor and acceptor type dopants into a silicon channel film using the process of ion implantation. As expressly noted by the Examiner, however, Chiang, et al., "fails to disclose the required fixed electrical charge manipulation" recited in claim 1. The Examiner thus refers to Makita et al.

Makita et al. relates to a thin film transistor which "includes an active layer and a first insulating film and a second insulating film sandwiching the active layer, wherein the overall polarity of fixed charges contained in the first insulating film is the reverse of the overall polarity of fixed charges in the second film" (col. 2, line 67 – col. 3 line 5).

The thin film transistor of Makita et al. is shown in Figs. 1A and 3D below (as annotated by applicant for clarity).

FIG. 1A

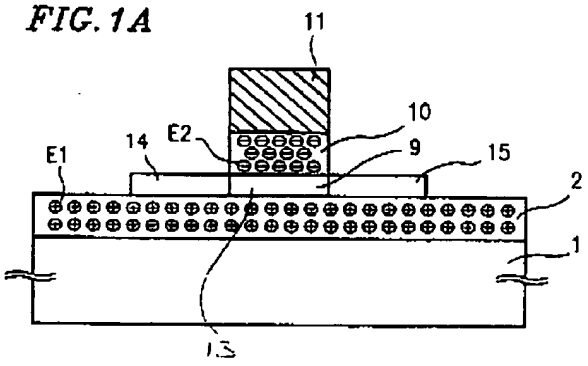
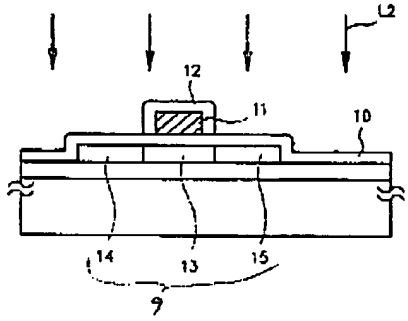


FIG. 3D



Figs. 1A and 3D are schematic representations of the thin film transistor of Makita et al. As such, the drawings show an active layer **9** of the transistor, the active layer including source and drain contact regions (**14** and **15**) and channel region **13**. As indicated, channel region **13** is sandwiched between insulating layer **2** (within which positive fixed charges **E1** are incorporated) and insulating layer **10** (within which negative fixed charges **E2** are incorporated). The fixed charges are **not** in the channel region.

In fact, Makita et al. specifically teaches against implanting n-type impurities or p-type impurities in the channel region of the transistor, noting that "the impurities implanted in the channel region dull the rising of a drain current in the subthreshold region during the operation of the MOS transistor, as well as increasing the leak current during the non-operation thereof" (col. 2, lines 28-34). As stated in MPEP § 2145.05, "It is improper to combine references where the references teach away from their combination." The Examiner's proposed reading of Makita et al. to teach fixed electrical charge density manipulation within the channel region thus cannot stand, and the rejection of claim 1 under 35 U.S.C. § 103(a) based on Chiang et al. in view of Makita et al. must be withdrawn. Furthermore, since claims 2-3 and 23 depend from claim 1, such claims are allowable for at least the same reasons as claim 1.

Claims 24-25

Claim 24 recites a thin-film transistor including source, drain, and gate electrodes, a dielectric insulator, and a deposited thin-film semiconductive channel, "where the semiconductive channel includes a first portion and a second portion, the first portion being doped differently than the second portion so as to achieve a desired variation in a gate threshold voltage required to turn on the thin-film transistor." Claim 25 depends from claim 24.

As recognized by the Examiner, and as discussed with respect to claim 1 above, Chiang et al. "fails to disclose the required fixed electrical charge manipulation" of the semiconductive channel. The Examiner thus relies on Makita et al. However, as also discussed above, Makita et al. reference actually teaches away from the introduction of fixed charges into the channel region. The rejection of claim 24 under 35 U.S.C. § 103(a) based on Chiang et al. in view of Makita et al. thus must be withdrawn. Furthermore, since claim 25 depend from claim 24, claim 25 is allowable for at least the same reasons as claim 24.

Claim 29

Claim 29 has been cancelled without prejudice, thus rendering the Examiner's rejection of claim 29 moot.

Claim 39

Claim 39 recites a transistor including source, drain, and gate electrodes and "a channel region having a portion doped with an impurity to change the fixed charge density within the portion relative to a remainder of the channel region."

As recognized by the Examiner, and as discussed with respect to claims 1 and 24 above, Chiang et al. "fails to disclose the required fixed electrical charge manipulation" of the channel region. The Examiner thus relies on Makita et al. to teach fixed charge manipulation of the channel region. However, as also discussed above, Makita et al. reference actually teaches away from the introduction of fixed charges into the channel region. Applicant thus asserts that the Examiner has failed to establish the *prima facie* obviousness of claim 39, and respectfully requests withdrawal of the rejection of this claim under 35 U.S.C. § 103(a) based on Chaing et al. in view of Makita et al.

Claim 40

Applicant has cancelled claim 40, without prejudice, thus rendering the Examiner's rejection of claim 40 moot.

Statement of Reasons for the Indication of Allowable Subject Matter

In the Office Action, the Examiner paraphrased applicant's claimed invention as part of the stated reasons for the indication of allowable subject matter. Applicant agrees with the Examiner's conclusions regarding the patentability of the allowed claims, without necessarily agreeing with or acquiescing in the Examiner's reasoning. In particular, applicant believes that the application is allowable because the prior art fails to teach or suggest the invention as claimed, independent of how the invention is paraphrased.

Conclusions

Applicant believes that this application is now in condition for allowance, in view of the above amendments and remarks. Accordingly, applicant respectfully requests that the Examiner issue a Notice of Allowability covering the pending claims. If the Examiner has any questions, or if a telephone interview would in any way advance prosecution of the application, please contact the undersigned attorney of record.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to Examiner N. Flynn, Group Art Unit 2826, Assistant Commissioner for Patents, at facsimile number (703) 872-9306 on March 21, 2005.

Christie A. Doolittle